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Time-Reversal Based Range Extension Technique for Ultra-wideband (UWB) Sensors and Applications in Tactical Communications and Networking

Technical Report (Quarterly)

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14. ABSTRACT

This technical report (quarterly) details the work for Office of Naval Research (ONR) by Tennessee Tech. The goal of this project—jointly funded by ONR, NSF, and ARO—is to build a general purpose testbed with time reversal capability at the transmitter side. The envisioned application is for UWB sensors and tactical communications in RF harsh environments where multipath is rich and can be exploited through the use of time reversal. The report summarizes the results for each of two major tasks: theoretical research and experimental testbed.

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Executive Summary

This technical report (quarterly) details the work for Office of Naval Research (ONR) by Tennessee Tech. The goal of this project—jointly funded by ONR, NSF, and ARO—is to build a general purpose testbed with time reversal capability at the transmitter side. The envisioned application is for UWB sensors and tactical communications in RF harsh environments where multipath is rich and can be exploited through the use of time reversal. The report summarizes the results for each of two major tasks. Specifically, the project can be broken into

- Task 1–Theoretical Research
- Task 2–Experimental Testbed

In the part of theoretical research, the central effort is to investigate the new approaches to leverage the testbed. In particular, environmental sensing seems be enabled by our time reversal testbed, since channel impulse response that is required for time reversal can be exploited for environmental sensing, simultaneously used for data communication. The physical phenomenon of diffraction for radio waves, such as holes and corners, seems to limit communication and sensing in harsh environments such as intra-ship, since the wavelengths of the time-harmonic radio waves possessed by a transient, short pulse are comparable with the characteristic sizes of the environments. For example, this is the case for a pulse of bandwidth from 700 MHz to 10 GHz. Experimental and theoretical investigation is being carried out to systematically understand this limitation for the system testbed.

In the experimental testbed part, progress in the second generation of the testbed—with time reversal—is described. At this moment of writing, the first generation (1G) of the testbed—without time reversal—is working at the PI's Lab, over the air with a bandwidth of more than 500 MHz. The second generation (2G) will be built upon the first generation. The primary modification is the arbitrary modulation waveform generation at the transmitter. For the 2G testbed platform, the analog-to-digital converter (ADC) and new Xilinx Virtex-5 board are working. The next milestone is to get the arbitrary waveform generator running. Then we can start system integration test.

Contents

Chapter 1

Introduction

Civilian and naval vessels have long been potential targets for criminal and terrorism activities. There are concerns that terrorists can ship various types of weapons of mass destruction (WMD) to international ports using commercial ships and their cargoes. One of the major steps in preparedness for such danger is reliable wireless communications both between the boarding party as well as effective ship-to-ship and ship-to-shore communications once the first sign of threat is detected. This need is made possible, only recently [1], with the advent of revolutionary ultra-wideband (UWB) technology [2, 3, 4, 5, 6, 7, 8, 9]. This proposed research is motivated for RF challenged environments such as hospital, coal-mine, intra-ship, intra-vehicle, intra-engine, manufacturing plants, assembly lines, nuclear plants, body area network sensors surrounded by vehicles and tanks, etc.

In the part of theoretical research, the central effort is to investigate the new approaches to leverage the testbed. In particular, environmental sensing seems be enabled by our time reversal testbed, since channel impulse response that is required for time reversal can be exploited for environmental sensing, simultaneously used for data communication. The physical phenomenon of diffraction for radio waves, such as holes and corners, seems to limit communication and sensing in harsh environments such as intra-ship, since the wavelengths of the time-harmonic radio waves possessed by a transient, short pulse are comparable with the characteristic sizes of the environments. For example, this is the case for a pulse of bandwidth from 700 MHz to 10 GHz. Experimental and theoretical investigation is being carried out to systematically understand this limitation for the system testbed.

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Several key lessons are learned from previous research carried out in this project:

- To further extend the range for networking and sensing, the design of modulation waveforms must be carefully selected, according to some criteria, for the transient pulse: The time-bandwidth product is often very small, fundamentally different from that of the narrowband system. A good criterion is to maximize the signal to noise ratio (SNR) measured at the point after the matched filter. The frequency selectivity of the channel [14], due to the huge bandwidth, will lead to the unique problem of pulse waveform optimization. For example,

when diffraction occurs for a path, this huge bandwidth will reduce the "space bandwidth" of the pulse that in return limits the capacity of the path channel. This happens too often in harsh environment where key holes and edge corners are necessary paths for communication and sensing. This diffraction-limited phenomenon is unique to a transient pulse.

- Another key understanding is that the effective channel enabled by time reversal can be treated "non-fading". This phenomenon of "non-fading", unique to UWB communication, arises from the extremely high resolution of a transient pulse—so almost all significant paths are resolvable in time, avoiding multipath fading. The system design will greatly simplified under this non-fading framework. Although this theoretical breakthrough is reached, the design principle and system parameters to exploit this new phenomenon are far from clear, and under investigation in this project.

- The above two fundamental mechanisms—diffraction and extremely high resolution—primarily explain the first successful UWB wireless communication within a ship [1]. For narrowband communicaiton, fading up to 90 dB will make communication difficult. A transient pulse, however, seems suitable for this kind of harsh envionments. For example, the diffracted pulse by a sharp edge is simply a semi-integral of the incident pulse waveform (multiplied by a constant energy attenuation factor), given by (2.1). Within a metal ship, only two propagation mechanisms exist: perfect reflection and diffraction. The geometric theory of diffraction (GTD) combined with geometric optics [10]- [13] is sufficient.

- Because thousands of paths are resolvable in time, time reversal is basic to a quasi-continuous-time impulse response of extremely long delay spread.

- The key UWB system design consists of two parts: (1) time reversal to deal with dense multipath; (2) the selection of UWB modulation pulse waveform—software defined or cognitive. From a information-theoretical viewpoint, the two parts, as a whole, form so-called "pre-coding".

- Multiple-input-multiple output (MIMO) takes advantages of spatial degrees of freedom to achieve multiplexing gain [16] [15]. The phenomenon diffraction, however, limits spatial degrees of freedom that in turn limits the capacity of the channel. The ultimate transmission data rate of a time reversal UWB system is limited by diffraction and multipath.

This three-year ONR project started in January 2007 and will end in 2009. This project was previously initiated by Army Research Office (ARO) and Army Research Laboratory (ARL), and picked up by ONR and National Science Foundation (NSF). Potential applications for Air Forces/NASA are under investigation, through collaboration with University of Tennessee Space Institute (UTSI) and Oak Ridge National Laboratory. One goal is to develop UWB technology that will be useful to Navy, Army and Air Forces (NASA). We also did experiments in coal-mine environments since Department of Labor has listed UWB technology as one of two key technologies for coal-mine communication and tracking.

The impact of this project is broad. This project is currently funded by NSF (ECCS-0622125, August 1, 2006-July 31, 2009, 1 PI, 1 co-PI, 2 PhD students). A Research Experiences for Undergraduates (REU) supplement of the project and additional supplement for International Research and Education in Engineering (IREE) have both been granted. Under the IREE program, two undergraduate students are doing research with the PI, and will go with the PI to Lund University (Sweden) for 3.5 months in the summer of 2008. Two PhD dissertations [15, 17] and three master theses have been written on UWB communication. Three PhD students, two master students, and two BS students (including one Hispanic female student), together with one R & D engineer, are working within the project. New PhD and master students are expected to join the team in the summer of 2008.

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Chapter 2

Environmental Sensing Enabled by Time Reversal Communications

UWB technology is promising for wireless sensor networking [1, 2, 3, 4]. Our picture of UWB impulse radio sensors has combined three functions: (1) communications and networking; (2) geo-location; (3) environmental sensing. The objective of this project is to exploit the dense multipath through time reversal transmission at the transmitter side. Time reversal transmission takes advantage of the extremely high resolution offered by using ultra-wideband pulses: Multipath can be resolvable, in the time domain, into a huge number of pulses—each pulse corresponds to a physical path. Compared with the transmitted pulse, each pulse of those pulses is often distorted in shape, delayed in time, and attenuated in amplitude.

A new approach is proposed in this report, to exploit the knowledge of time reversal transmission: The channel impulse response—static with no fading—is available at the transmitter side (and easily available at the receiver side, if needed). Time reversal transmission is an enabler technology as our point of departure, and will enable a variety of new schemes. For example, in the front of better communication and networking, pre-coding can be enabled to provide higher data rates or save the transmitted sensor energy. Here, environmental sensing is proposed to be implemented in the testbed, exploiting the unique transceiver structure of time reversal transmission.

2.1 Environmental Sensing Exploiting Channel Impulse Response

For both military and civilian applications, devices are needed to "see" through metal walls, into enclosed spaces, and around (impenetrable) corners to locate and track concealed persons. For example, intra-ship and fleet-to-fleet communication often encounters non-line-of-sight (NLOS) diffraction by metal edges, such as doors, windows, hall-way edges, stairs, etc. Motivated by these applications, some theoretical and experimental work has been performed. The idea is to leverage the platform for time reversal transmission. Geo-location will be implemented using the current hardware architecture (but requires a number of nodes). On the other hand, environmental sensing has been not reported in our previous (quarterly) reports. Here, we will touch only the preliminary results: most work is in the stage of theoretical research. Experimental work has recently started.

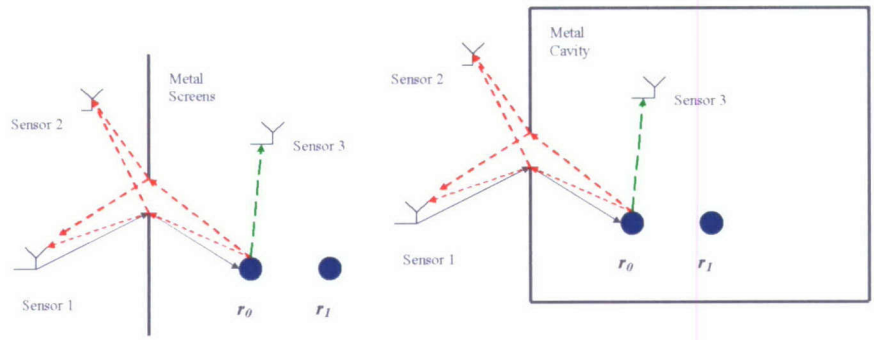


Figure 2.1: Illustrate of Impulse Radio Communication and Environmental Sensing. (a) Slit composed of two half-plane edges—around corners; (b) Cavity with a slit—"see" through enclosed spaces.

2.1.1 Model and Formulation

To illustrate the underlying principle behind environmental sensing, let us consider the scenarios in Fig. 2.1: (a) slit composed of two half-plane edges—around corners; (b) cavity with a hole—"see" through enclosed spaces. If the metal slit is sufficiently wide, i.e., the width size of the slit is comparable with the wavelengths of the used pulse, the movement of the target can be tracked, in principle.

Let us denote the width size of the slit by b and the wave length λ. If b/λ is large enough, both communication[1] and sensing are possible. The slit can be, roughly, viewed as a superposition of two half-plane edges. For an incident, transient pulse $x(t)$, the edge diffraction is equivalent to the fractional integral of the incident pulse. That is, the output pulse due to the incident pulse is expressed as

$$y(t) = \frac{1}{a} I^{\alpha} x(t), \quad \alpha = 1/2 \tag{2.1}$$

where a, independent of time t, is an energy attenuation factor, caused by the presence of the metal edge, as a function of distance from the edge, and incident and observation angles. The fractional integral of the order α is defined as

$$I^{\alpha} f(x) \equiv \frac{1}{\Gamma(\alpha)} \int_0^x \frac{f(t)}{(x-t)^{1-\alpha}} dt, \quad x > 0 \tag{2.2}$$

where $\alpha > 0$ is a real value. This integral is also called Riemann-Liouville fractional integral. This connection is made in [5].

The free space propagation between the edge and the sensor will cause pulse amplitude attenuation and time delay, but no pulse shape change. This kind of propagation, unlike edge diffraction, will not cause pulse waveform optimization.

[1] Both networking and communication are possible. For brevity, only communications is mentioned in the rest of the report, when both are meant.

2.1.2 Physical Mechanisms for Environmental Sensing

In Fig. 2.1(a), a transient pulse is transmitted from Sensor 1. It propagates, through air, to reach two metal edges and is diffracted by the two edges. Two pulses—attenuated and fractional-integrated versions of the incident pulse—will be formed, immediately after the edge diffraction. The two diffracted pulses propagate to the metal target—e.g. a living person—located at $\mathbf{r}_0$. A human being can be treated as salt waters that are good metals to electromagnetic pulses. Currents are excited on the surface of the metal target. According to Huygens' principle, the target can be regarded as equivalent antennas—reradiating the captured energy from its surface.

When a transient pulse incident on a target, e.g., human being modeled by a metal cylinder in Fig. 2.2(a), two pulses are generated from this diffraction process in the shadowed region, see Fig. 2.2 for illustration [6]. An additional pulse will be generated if the observation sensor is located outside the shadowed region. We know, one impulse will generate two pulses by the two edges of the slit Fig. 2.1(a). If we transmit one short pulse from Sensor 1, by combining the two mechanisms—slit and cylinder, we can expect the Sensor 3 to detect six pulses—if Sensor 3 is far enough from the slit, so the diffracted pulses will be too weak to be detected.

The six pulses will back propagate and transmit through the slit again. Twelve pulses will be generated by the slit. As a result, Sensor 1 and Sensor 2 will detect these 12 pulses. The key advantage of transient UWB pulses over the narrowband, sinusoidal signals is that the former can be ***resolvable in time***, to avoid multipath fading suffered by the narrowband signals. We can take advantage of this key feature for environmental sensing.

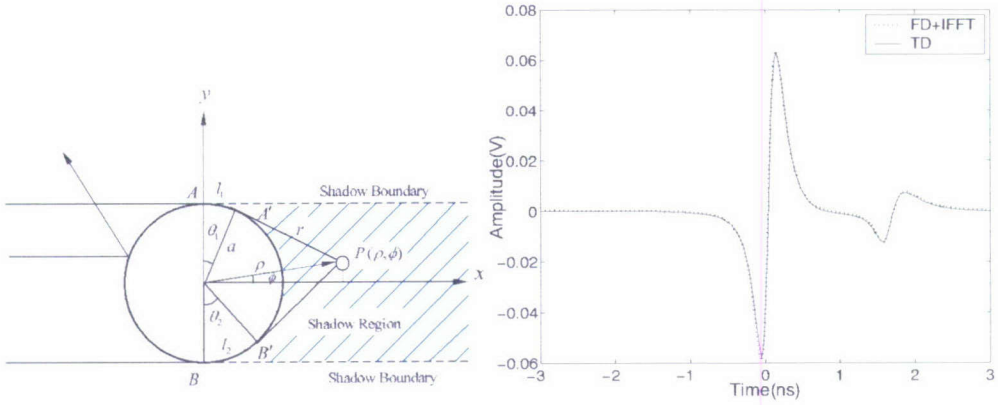
In the above physical picture, the target is located at position $\mathbf{r}_0$. What happens, if the target is located at position $\mathbf{r}_1$? Since the different arrival timings of these 12 pulses are sensitive to the change of the target location, the small distance change, $|\mathbf{r}_1 - \mathbf{r}_0|$, from $\mathbf{r}_0$ to $\mathbf{r}_1$, will cause a detectable difference in the timings of these 12 pulses detected by Sensor 1 and 2 (or six pulses for Sensor 3). These physical mechanisms are the basis for the new systems for environmental sensing.

Another advantage of the transient pulses is not to suffer from, but to exploit the harsh environments for environmental sensing. Let us consider Fig. 2.1(b) for example. Recall that, two diffracted pulses and one reflected pulse are generated from the cylinder (target). These three pulses will be bounced by the walls of the cavity to form so-called multipath pulses. In a typical cavity, thousands of resolvable pulses can be detected within a metal cavity. When the target changes a position, this distance change make a detectable difference to all these bounced pulses. As a result, the cavity greatly adds the capability of the system to "sense" the small change in distance (target movement). The key observation is that the pulse must be sufficiently short so the difference caused by the position change can be resolvable in time.

2.1.3 Pulse Waveform Optimization through Singular Value Decomposition of Fractional Integral

In the example of Fig. 2.1, it is seen that edge diffraction is a basic mechanism for both communication and sensing. A question naturally arises from this observation: What is the optimum pulse waveform to propagate across the edge? The optimum criterion can maximize either pulse energy and data capacity across the edge. The whole theory is being lectured [7], and will be documented in next (quarterly) report.

This theory provides a new analytical formalism to design optimum pulse waveform that can be implemented in the testbed under development in this funded project.

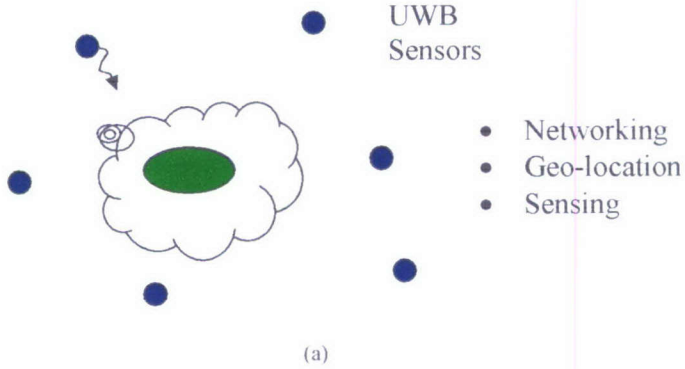


(a) (b)

Figure 2.2: The incident plane wave is diffracted by a metal cylinder [6] at observation point $P(\rho, \phi)$. The solid curve labeled by "TD" for time domain (TD) is obtained by convolving the incident pulse with the impulse response. The "FD+IFFT" curve is obtained by applying inverse fast Fourier transform (FFT) on the corresponding frequency domain (FD) result.

2.1.4 Potential Applications

As pointed out previously, we envision UWB sensors with three functions: (1) high-speed communication and networking; (2)geo-location; (3) environmental sensing. See Fig. 2.3 for illustration of distributed sensors. Since channel impulse response is already available for the purpose of communication and networking, it is natural to exploit this information for environmental sensing. The channel impulse response recorded for each sensor can be transfered, via the communication capability of the sensors, to a center for data fusion (centralized processing). One application is target detection and identification.



(a)

Figure 2.3: Distributed Sensor Applications.

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Chapter 3

Testbed Development Overview

Recent progress and work plan will be reported in the following.

After a few years of accumulative work on UWB radio, currently we have had a working UWB communication system (1G, 1st generation) with OOK modulation and energy/envelop detector. Some measured results of this system are reported in this report.

The current ONR project benefits from our previous work on 1G testbed. Different from the 1G system, the newly designed system is capable of transmitter-side pre-processing, and relies on Virtes-5 FPGA—a newer version Xilinx FPGA—to achieve high sampling rate. Compared to a regular communication system, one of many features of the testbed under development is arbitrary waveform generation at a sampling frequency over 500 MHz. We have, recently, successfully generated desired waveforms at sampling frequency 1 GHz, using an isolated D/A device. The next urgent work is to get the D/A connected with both the digital back-end and the analog front-end, which will involve a few challenges such as high-speed digital connection and Virtex-5 FPGA based back-end implementation.

This testbed development project has a number of technical aspects: system design, digital back-ends, mixed signal, RF front-ends, and system integration. The project is in progress, as planned, and is on the way to the next milestone (see milestones list in Table I). The goal for next few months is to achieve an over-the-air UWB time-reversal transmission. The pressure will be on Virtex-5 based digital back-end implementation, high-speed connection, RF front-end and system integration.

TABLE I. Milestones

Stable Architecture	8/2007
Time Reversal System with Cable	1/2008
Time Reversal System over the Air (Some Field Test)	6/2008
Fully Functional UWB System with Time reversal	1/2009
System Field Test	6/2009
Potential Technology Transfer to US Navy	12/2009

Chapter 4

High Speed Data Interface

4.1 High Speed Analog to Digital Converter

The MAX108, a 1.5 GHz flash ADC, is employed to convert the baseband signal (analog signal) into digital domain. A baseband amplifier between the low pass filter following the square law detector and ADC is necessary for signal conditioning. The ADC shown in Fig. 4.1 employs a fully differential 8 bits quantizer and a unique encoding scheme to limit metastable states, with no error exceeding 1 LSB max. To facilitate a lower rate digital interface, the ADC features an on-chip, selectable 8:16 positive-referenced emitter-coupled logic (PECL) compatible output demultiplexer that reduces the output data rate to one-half the sampling clock rate. The PECL outputs can be operated from any supply between +3 V and +5 V for compatibility with +3.3 V or +5 V referenced systems. This demultiplexer has internal reset capability that allows multiple MAX108s to be time-interleaved to achieve higher effective sampling rates. The full scale analog input range of the MAX108 is ±250 mV for differential or single-ended use. In addition, this ADC also features an on-chip +2.5 V precision voltage reference. The number of bits of the ADC used by the FPGA can be dynamically adapted to the environment; reducing the number can downscale the FPGA resource usage and total power assumption. A single-data-rate (SDR) interface with a FIFO memory is implemented in FPGA to receive data from the ADC.

The MAX108 evaluation board shown in Fig. 4.2 is integrated into the testbed to perform the analog-to-digital conversion. The evaluation board makes it easier to include the ultra-high-speed ADC in the prototyping system. The differential signaling is required for the input analog signal and the sampling clock. The sampling rate is up to 1.5 GHz, which is determined by frequency of the external sampling clock. A sinewave with power level of +4 dBm is fed into the CLK+ port on the ADC board as the sampling clock. The CLK- port on the ADC board is grounded via a 50 Ω SMA terminator. The input analog signal is connected to the port VIN+ on the ADC board through a 50 Ω SMA coaxial cable. The VIN- port on the ADC board is grounded vis a 50 Ω SMA terminator. Since the input signal range of the ADC board is from -250 mV - +250 mV, a 10 dB attenuator is placed between the output of RF board and the input of the ADC board. A total of 16 pairs of PECL output signals are connected to the FPGA development board via a ADC/FPGA interface board. The most significant 4 bits of ADC outputs are used in the FPGA design in order to achieve a balance between performance and complexity.

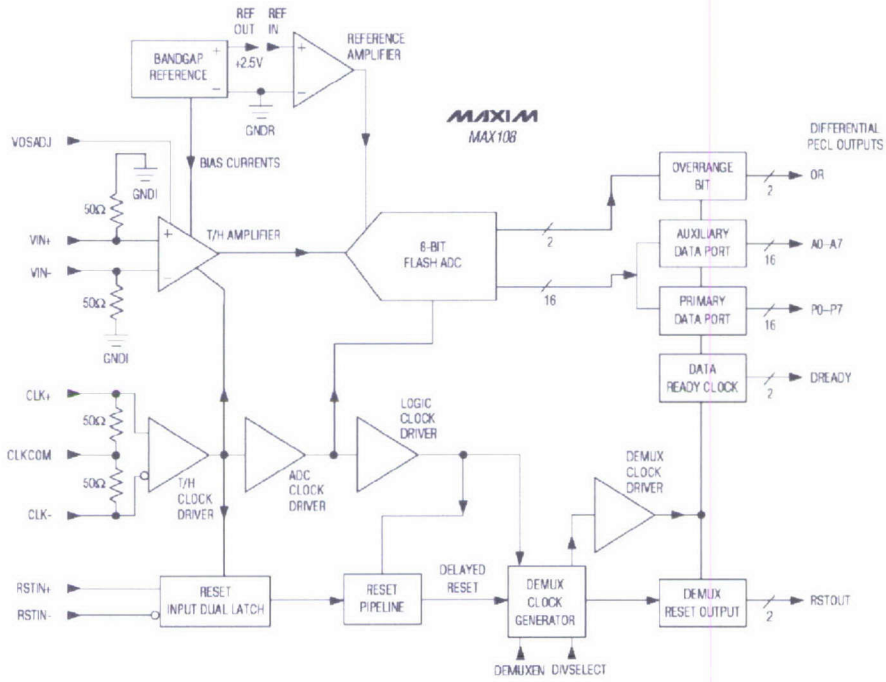

Figure 4.1: MAX108 simplified function diagram.

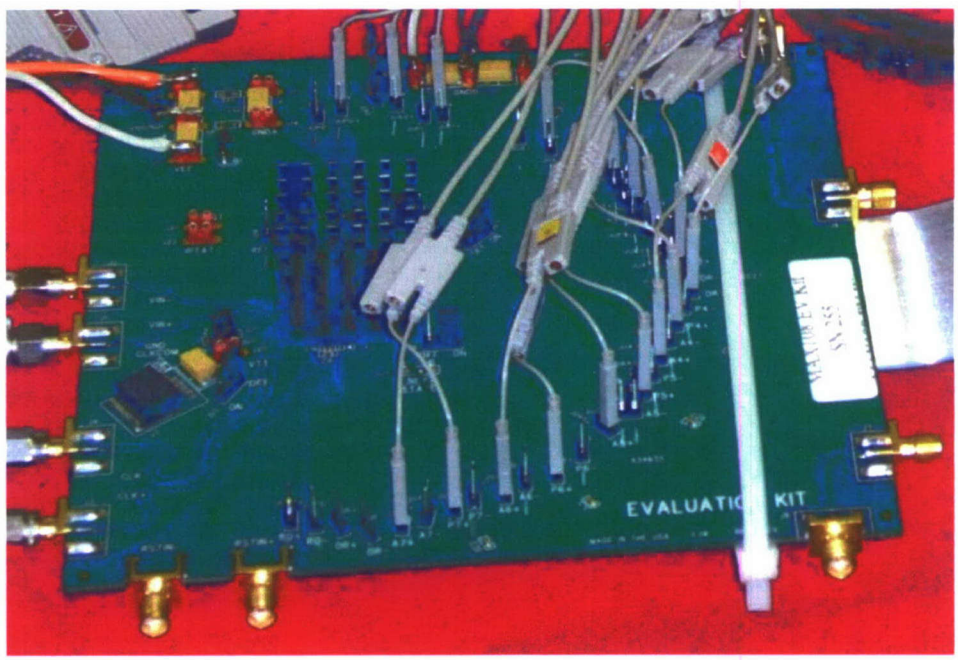

Figure 4.2: MAX108 evaluation board.

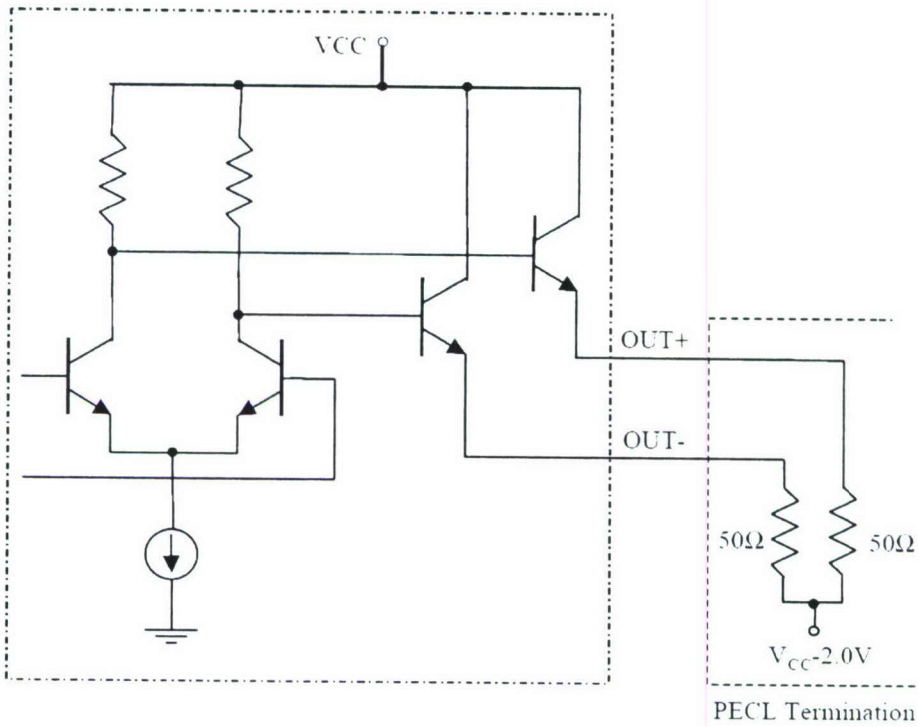

Figure 4.3: PECL output structure.

4.2 Positive Emitter Coupled Logic

PECL is a commonly used ultra-high speed data transmission interfaces for high performance, low power, and good noise immunity. PECL originates from emitter coupled logic (ECL), but uses a positive power supply.

The PECL output shown in Fig. 4.3 consists of a differential pair that drives a pair of emitter followers. The output emitter followers operate in the active region, with DC current flowing at all times. This increases switching speeds and helps maintain fast turn-off time. The proper termination for a PECL output is 50 Ω to VCC - 2 V. At this termination, both OUT+ and OUT- will typically be VCC - 1.3 V, resulting in a DC current flow of approximately 14 mA.

When the power supply is +3.3 V, PECL is commonly referred to low-voltage PECL (LVPECL). For many FPGAs, LVPECL transmitter and receiver are embedded in the device for high-speed data transmission. Virtex-II FPGA's I/Os are designed to comply with the specifications for 3.3 V LVPECL. The termination for an embedded LVPECL receiver, suggested by Xilinx, is shown in Fig. 4.4.

4.3 High Speed Interface between ADC and FPGA

For the design of the high-speed interface between ADC and FPGA, signal integrity has become a critical issue. Many signal integrity problems are electromagnetic phenomena in nature and hence related to the EMI/EMC. There

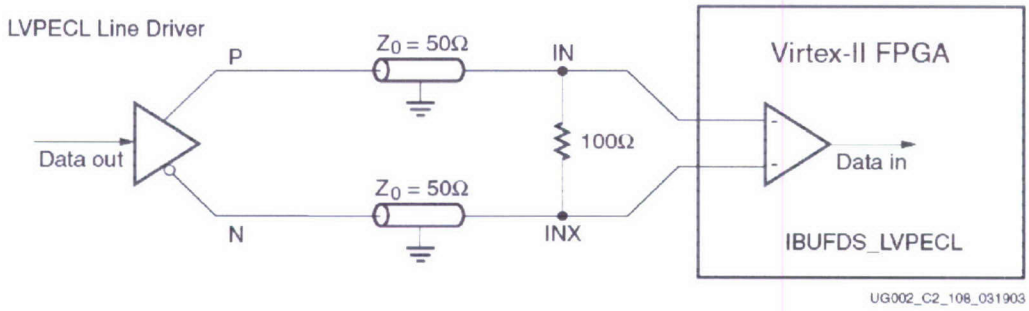

Figure 4.4: FPGA's LVPECL receiver termination.

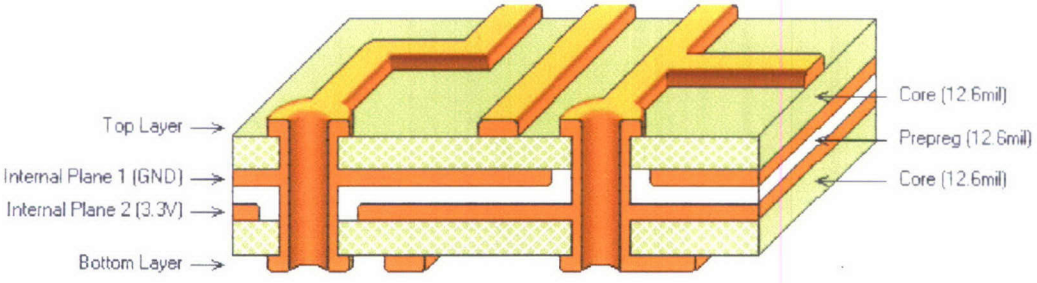

Figure 4.5: Interface board PCB layer stack.

are two concerns for signal integrity: the timing and the quality of the signal. Signal timing mainly depends on the delay caused by the physical length of trace that the signal must propagate. Signal waveform distortions can be caused by reflection, cross talk, and power/ground noise. An interface has been carefully designed to solve the signal integrity issue. PCB layout, transmission line terminations, and connection cables are three major considerations in the high speed ADC/FPGA interface design.

Since the signal frequency is high, every PCB trace must be analyzed as a transmission line. Its series resistance and parallel conductance can generally be ignored, but series inductance and parallel capacitance per unit length are important parameters. Any signal transition (rising or falling edge) travels along the trace at a speed determined by the incremental inductance and capacitance. For an outer-layer trace (air on one side), the propagation delay is 55 ps/cm. For an inner-layer trace (FR4 with $\epsilon = 4.5$ on both sides), the propagation delay is 70 ps/cm. The signal propagation delay can be calculated based on information above.

A 4-layer PCB board is designed and fabricated to have 50 Ω characteristic impedance for each trace. The PCB layer stack is shown in Fig. 4.5. As shown in Fig. 4.6, for each pair of LVPECL signals, the traces are designed to have same length such that the positive and negative signals experience same delay.

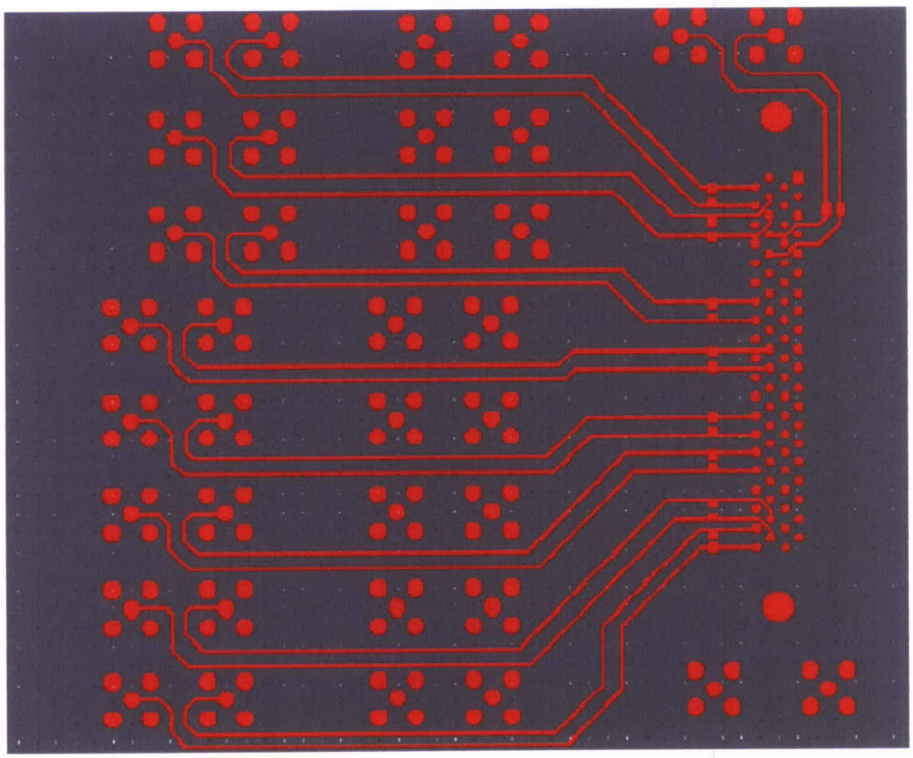

Figure 4.6: Interface board top layer layout.

An important parameter is the characteristic impedance Z_0 defined as the voltage-to-current ratio at any point along the transmission line. It is determined by the ratio w/d, where w is the trace width, d is the distance above the ground or VCC plane. For an outer layer trace (microstrip), Z_0 = 50 Ω when $w = 2 * d$. For an inner layer trace between two ground or VCC planes (stripline), Z_0 = 50 Ω when $w = 0.6 * d$. Most signal traces fall into the range of 40 - 80 Ω. At any trace-impedance discontinuity, all or part of the signal is reflected back to the origin.

If the far end is resistively terminated with R = Z_0, there is no reflection. If, however, the end is open, or loaded with only a CMOS input, then the transition doubles in amplitude, and this new wave travels back to the driver, where it may be reflected again, resulting in the familiar ringing. Such ringing has a serious impact on signal integrity, reduces noise margins, and can lead to malfunction. A way to avoid reflections and ensure signal integrity is a proper termination. It can be observed the signal swing is reduced significantly with the presence of proper termination in Figs. 4.7 and Fig. 4.8.

Crosstalk can happen when two signals are routed closely together. Current through one of the traces creates a magnetic field that induces current on the neighboring trace, or the voltage on the trace couples capacitively to its neighbor. Crosstalk can be accurately computed by

$$Peak\ Crosstalk\ Voltage = \frac{\delta V}{1 + (d/h)^2} \tag{4.1}$$

where δV is the voltage swing, d is the distance between traces, and h is the spacing above the ground plane. The distance between two adjacent traces in the ADC/FPGA interface board are selected carefully in order to prevent from a false transition. In addition, SMA coaxial cables are used to transmit high speed digital signals from the ADC board to the interface board.

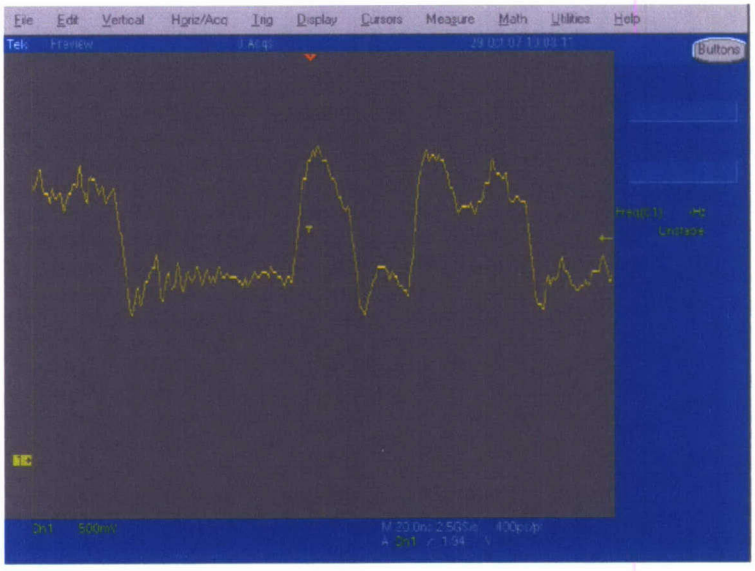

Figure 4.7: Signal waveform with proper termination.

Figure 4.8: Signal waveform without proper termination.

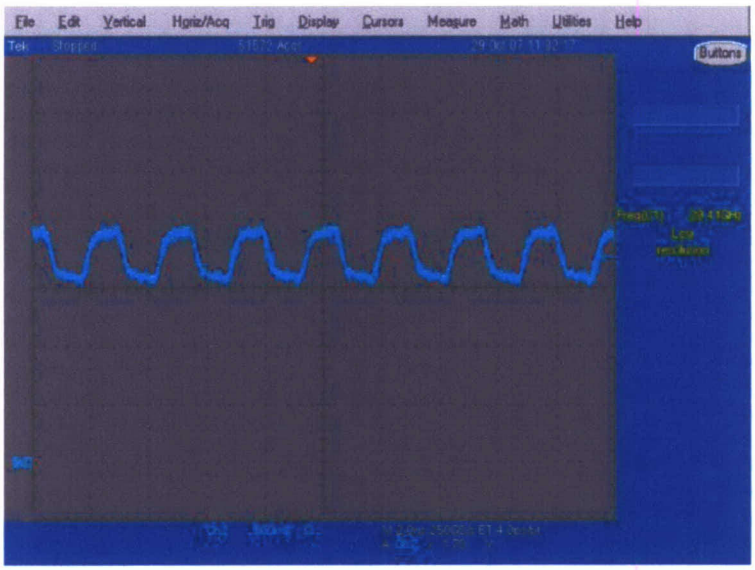

Figure 4.9: Clock waveform.

In the testbed, a 800 MHz clock is employed as the ADC sampling clock, so the corresponding ADC output signals have maximum frequency of 400 MHz. The interface solution is to make a ADC/FPGA interface board which is plugged into the FPGA development board, then the ADC board and the ADC/FPGA interface board are connected through 50 Ω SMA cables. The interface solution can support signals with frequency of up to several GHz. A clock signal waveform and a data signal eye diagram, measured at a FPGA input pad, are shown in Fig. 4.9 and Fig. 4.10, respectively.

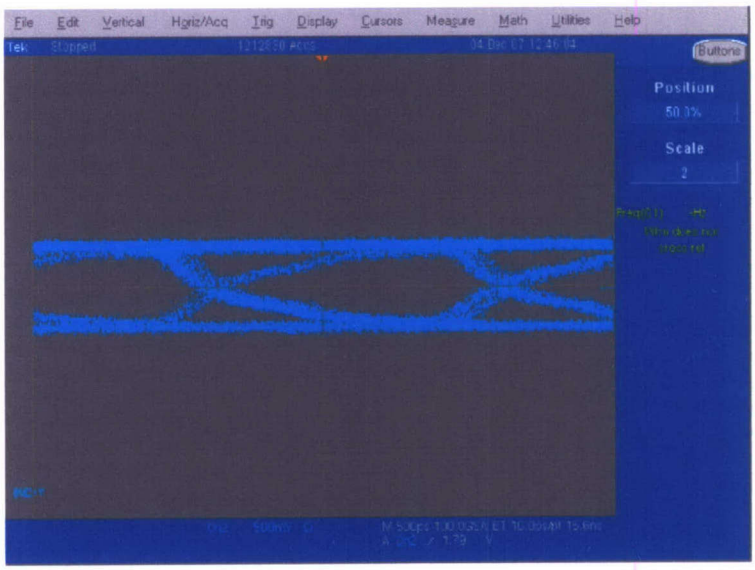

Figure 4.10: Data eye diagram.

Chapter 5

FPGA Consideration - Virtex-5

High-speed signal processing is strongly required in our UWB test-bed development. This ability is provided by the FPGA based digital back-end. Xilinx Virtex-2 FPGA chips have been employed in our previous UWB test-bed, supporting processing speed up to 400 Mb/s. In our current version of UWB test-bed, the claimed features include arbitrary waveform generation which has to rely on high-speed parallel signal processing. Thanks to recent advance in semiconductor technology, a newer family of FPGA platform, Virtex-5 family, has been developed by Xilinx and is now commercially available. Compared to Virtex-2, the Virtex-5 has more logic resources with much stronger processing ability, while consumes more than 35% less power. The Virtex-5 family is built upon the industry's most advanced 65-nm triple-oxide technology, breakthrough new ExpressFabric technology and proven Advanced Silicon Modular Block (ASMBL) architecture. It offers extremely good solution for addressing high-performance logic designs, high-performance DSP designs, and high-performance embedded systems designs with unprecedented logic, DSP, hard/soft microprocessor, and connectivity capabilities.

We choose Xilinx Virtex-5 FPGA device model, XC5VLX110T-3FFG1136CES, to implement all base-band processing in our new system, shown as Fig. 5.1. Xilinx product of XC5VLX110T FFG1136 prototype platform. The model was chosen to host our Virtex-5 device, as shown in Fig. 5.2. The platform is optimized for high-performance logic with low-power serial connectivity and high speed, which is needed in our system. Based on the device and the platform, we will greatly benefit from the following features:

- 550 MHz clock technology, up to 12 Digital Clock Managers (DCM) and one PLL; 550 MHz, 36 Kbit block RAM/FIFOs would enable our UWB system work at a speed as high as 1 Gb/s.
- 1.0 V core voltage, 1.2 to 3.3V I/O operation, Virtex-5 offers a 35% to 40% reduction in dynamic power

Figure 5.1: Virtex-5 XC5VLX110T-3FFG1136CES

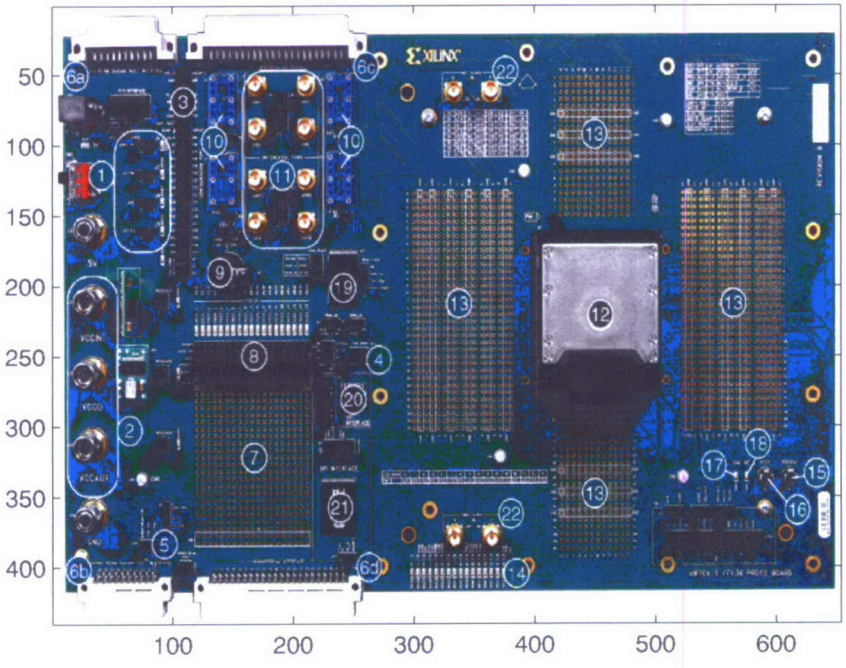

Figure 5.2: Detailed Description of Virtex-5 LXT/SXT Prototype Platform Components

consumption over the previous generation of FPGAs while keeping static power consumption at the same level.

- Up to 160 x 54 Configurable Logic Blocks (CLB) with 110,000 logic cells. Such abundant resources will sufficiently meet our system's requirements since all base-band processing and controlling functions need to be implemented in FPGA.
- Up to 640 user I/O, each with high performance SelectIO technology, working at 1.2 Gb/s LVDS (differential pairs) and 800 Mb/s HSTL & SSTL (single ended).This would enable high-speed connection between FPGA and other boards and devices, such as high speed D/A and A/D converters in our new UWB test-bed.
- Power-optimized high speed serial transceiver blocks for enhanced serial connectivity, working at 100 Mb/s to 3.2 Gb/s, would make a huge number of data be downloaded to FPGA at a high speed, since there would be huge estimated channel information needed to be processed at digital back-ends.
- Advanced DSP48E slices, featuring 25-bit x 18-bit two's complement multiplier and optional pipeline stages for enhanced performance and optional 48-bit accumulator. This would make it possible to implement complex algorithms in FPGA, for example, synchronization at the receiver side.

Other than the features mentioned above, there are many other advantages for Virtex-5, such as hard-coded PCI Express compliant integrated endpoint block, ChipSynch-support networking/telecommunications interfaces up to 1.25 Gb/s, tri-mode 10/100/1000 Mb/s Ethernet Media Access Controllers (MAC), etc.

All these features allow us to build the highest levels of performance and functionality into FPGA-based system. Xilinx software ISE foundation with XST synthesizer will be used for design synthesis and implementation.

Chapter 6

Arbitrary Waveform Generator

In the transmitter side of testbed, Xilinx Virtex-5 LXT Prototype Platform and Fujitsu DK86064 DAC Evaluation Kit are employed to build the arbitrary waveform generator. This arbitrary waveform generator can generate the continuous baseband waveform for general purpose of communication or remote sensing. The diagram of the arbitrary waveform generator is shown in Fig. 6.1.

The Virtex-5 Prototype Platform allows designers to investigate and experiment with the features of Virtex-5 FPGAs. In the testbed, the platform board's mounted ZIF socket hosts Virtex-5 FPGA in FF1136 package. Thanks to 550 MHz clock technology, Virtex-5 FPGA in conjunction with high-speed DAC can be used to generate the arbitrary waveforms of bandwidth over 500 MHz. The functionalities in the Virtex-5 FPGA is shown in Fig. 6.2. The baseline transmitter side module generates sequences of 1 and 0 chips at chip rate 25 Mcps. Discrete-time waveform is generated by the waveform generator module in the FPGA based on chip values and the pre-loaded waveform template; the discrete-time waveform is then fed to the DAC via a high-speed connection bus.

The DK86064 DAC Evaluation Kit allows users to evaluate and demonstrate the different operational modes of MB86064 digital to analog converter. In the testbed, the DK86064 DAC Evaluation Kit is connected to the Vitex-5 Prototype Platform and MB86064 converts the digital domain waveform to the analog domain waveform in the baseband. Fujitsu DK86064 DAC Evaluation Kit can support the input data with 1Gsps sampling rate and 14-bit resolution, but waveform generator module in FPGA is designed to generate two-branch data with 500 MHz sampling rate and 7-bit resolution in parallel. Data from one branch are the even samples of the original waveform data and are fed to DAC through port A; data from the other branch are the odd samples of the original waveform

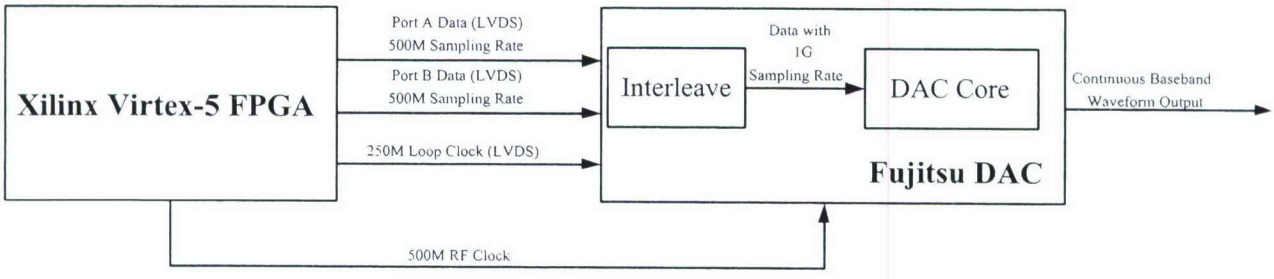

Figure 6.1: The diagram of the arbitrary waveform generator in the transmitter side.

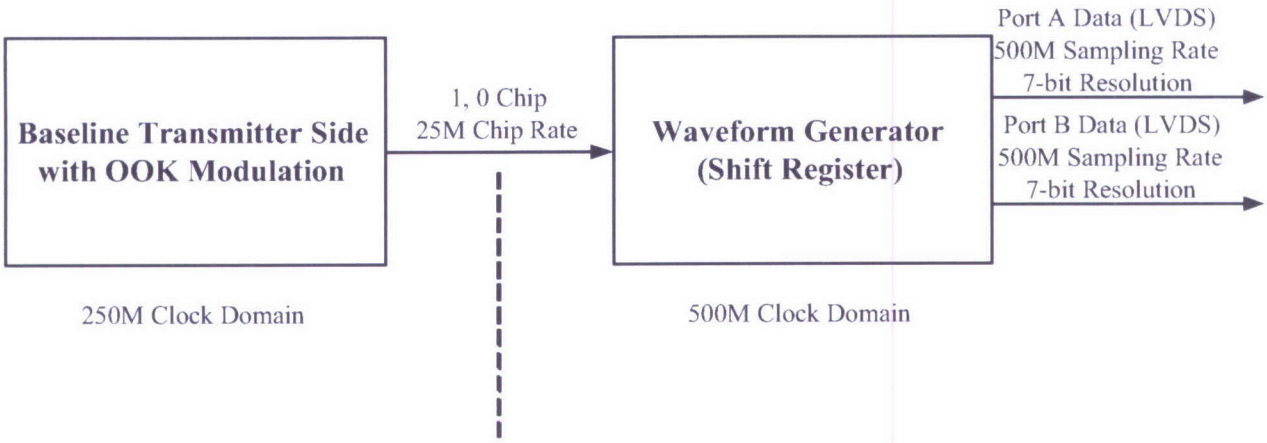

Figure 6.2: The functionalities in the Virtex-5 FPGA.

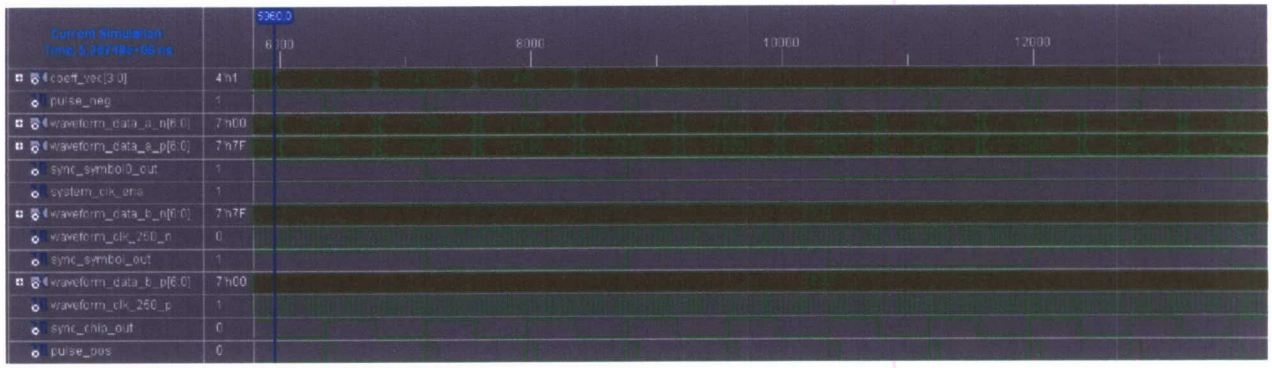

Figure 6.3: The output of waveform generator module in FPGA.

data and are fed to DAC through port B. DAC can interleave the date from two ports via waveform memory module (WMM). For testing waveform generator module, if the time duration of the waveform template is 160 ns, the shape is the unit impulse with the value of 1111111 at the 2^{nd} sample and the value of the input chip is 1, then the output of waveform generator module is shown in Fig. 6.3.

In order to know the functionalities and mechanisms of the DK86064 Evaluation Kit, we test it in the following way. A single-ended clock from signal generator is connected to SMA CLK (J3). The signal level of the clock is 10 dBm and the frequency of the clock is 500 MHz. The single-ended analog outputs on SMAs IOUT_A (J6) and IOUT_B (J1) are connected to digital phosphor oscilloscope (DPO). PC USB Programming Cable is connected to CONTROL I/F header (PL1). The power supply cable is connected to POWER header (PL6) with correct orientation. PC Programming Software is installed and operated to configurate the DAC. In the test, waveform data are downloaded to WMM in MB86064 from PC. Specifically speaking, a sine waveform with length of 1024 points is downloaded to RAM A in WMM and then is routed to DAC A; while a ramp waveform with length of 1024 points waveform is downloaded to RAM B in WMM and then is routed to DAC B. For the software configuration, the first step is to program the WMM registers according to the test requirements and generate the WMM register settings file reg_wmm.txt. The content of the WMM register settings file is shown in Table 6.1. The second step is to program the DAC registers and download the default DAC register settings file MB86064_ab_on_and_wmm_clk_on.txt. The content of the DAC register settings file is shown in Table 6.2. When the DAC register settings file is downloaded,

Table 6.1: The content of the WMM register settings file.

Register address	Register value
0x1b2	0x0
0x1c3	0x1c0
0x1c4	0x80

Table 6.2: The content of the DAC register settings file.

Register address	Register value
0x0	0x10
0x10	0x0
0x11	0x33
0x20	0x0
0x21	0x33
0x12	0x43f800
0x22	0x43f800

the WMM register settings file will also be downloaded automatically. The last step is to load RAM A, load RAM B and synchronize RAMs. Fig. 6.4 and Fig. 6.5 show the waveforms from DAC A and DAC B in DPO.

In the testbed, the connection between the Virtex-5 Prototype Platform and the DK86064 DAC Evaluation Kit is the important issue because of high sampling rate of the signal. Two SMA data adapters connecting to the DK86064 DAC Evaluation Kit are bought from Fujitsu and each adapter can provide 16 pairs of SMA ports in LVDS standards. Additional work is needed to build a physical interface at FPGA side. Data presented to the DAC core should be 14-bit unsigned binary, where bit 14 is the most significant bit (MSB) and bit 1 is the least significant bit (LSB). Although the DAC has a 14-bit resolution, it is not necessary to use up all of the bits. 7 bits (from bit 8 to bit 14) are actually used, which is quite sufficient from performance point of view. Table 6.3 shows the relationship between the SMA ports to be used in the adapters and pins in the data headers of the DK86064 DAC Evaluation Kit. The output of the DK86064 DAC Evaluation Kit is connected to the quadrature modulator which has the capability of converting complex modulated signal from baseband to RF.

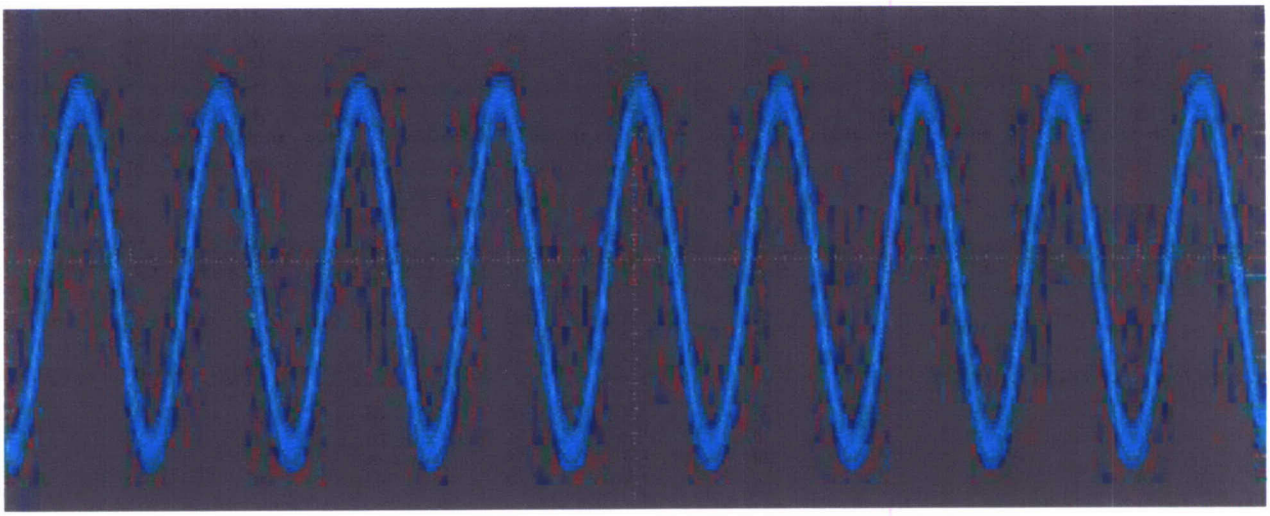

Figure 6.4: The output of DAC A.

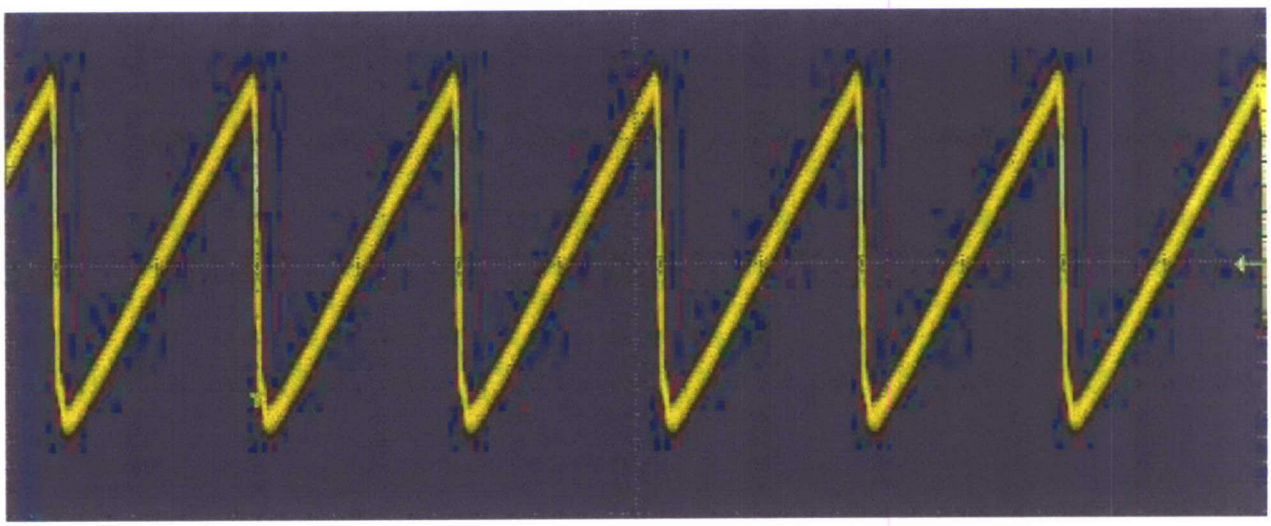

Figure 6.5: The output of DAC B.

Table 6.3: The relationship between the SMA ports in the adapter and the pins in the DAC.

SMA Port index	Pin index	Pin Location
J66	B8	PL5
J67	X_B8	PL5
J68	B9	PL5
J69	X_B9	PL5
J70	B10	PL5
J71	X_B10	PL5
J72	B11	PL5
J73	X_B11	PL5
J74	B12	PL5
J75	X_B12	PL5
J76	B13	PL5
J77	X_B13	PL5
J78	B14	PL5
J79	X_B14	PL5
J82	A8	PL3
J83	X_A8	PL3
J84	A9	PL3
J85	X_A9	PL3
J86	A10	PL3
J87	X_A10	PL3
J88	A11	PL3
J89	X_A11	PL3
J90	A12	PL3
J91	X_A12	PL3
J92	A13	PL3
J93	X_A13	PL3
J94	A14	PL3
J95	X_A14	PL3
J96	LPCLK_IN	PL3
J97	X_LPCLK_IN	PL3

Chapter 7

PC-Based System Testing Architecture and Its Applications

In this chapter, we propose a PC-based system testing architecture for our Time-Reversal (TiR) UWB testbed. With the proposed architecture, we can control other devices in the testbed and finish system testing via one PC. Various testing applications that can be supported by this architecture are described.

7.1 PC-Based System Testing Architecture

As reported in the quarterly report in October 2007, it is necessary and efficient to use PC to initialize and change FPGA settings during run-time. Data acquisition (DAQ) device and Visual C are used to accomplish these tasks. Now, we extend this idea to an overall testing control of the testbed. The architecture is demonstrated in Fig. 7.1.

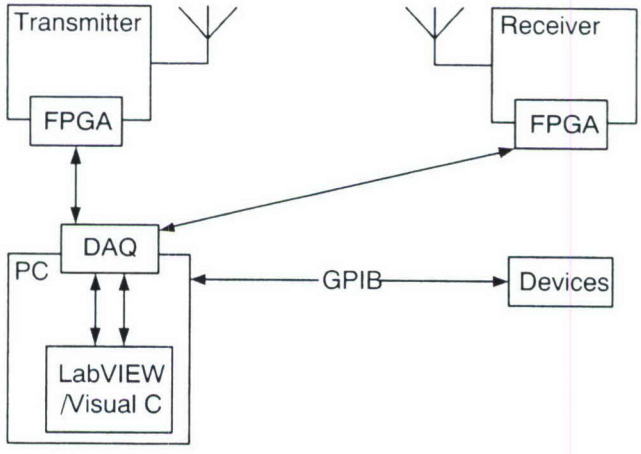

Figure 7.1: PC-based system testing architecture

This architecture supports communications between PC and measurement devices, such as FGPA, digital sampling oscillator (DSO), vector network analyzer (VNA) and spectrum analyzer (SA). DAQ is used to connect PC and

FPGA. GPIB bus is responsible for the connection between PC and other devices. LabVIEW is used as the virtual instrument (VI) software for process the data and manage the communications between devices. All data flows are two-way. Many applications can be built upon this architecture.

7.2 Application 1: Time Reversal Test

In our 2nd generation TiR testbed, the transmitter side needs channel side information (CSI). The receiver should first perform certain channel estimation algorithm and then transmit CSI to the transmitter through a feedback link. Since implementation of algorithms in FPGA is time-consuming, we should verify them before implementation. This task can be accomplished by setting up an alternative reverse link with our proposed architecture, as depicted in Fig. 7.2. First, DSO samples the received signal and transmit it to PC through GPIB bus. Then, the algorithms are performed using LabVIEW to obtain CSI. Finally, CSI is transmitted to FPGA through DAQ. As a result, different algorithms can be verified and compared before FPGA implementation.

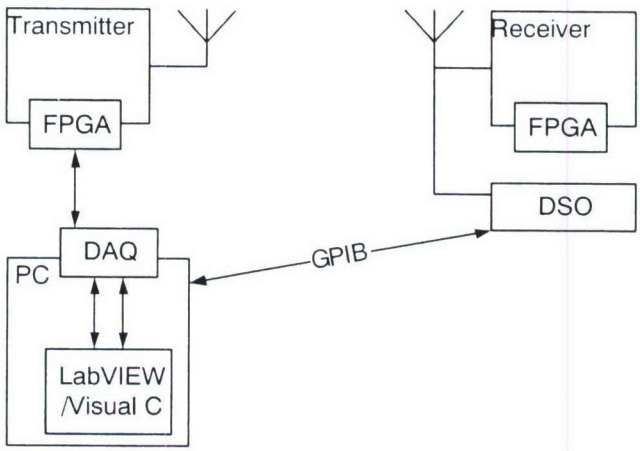

Figure 7.2: Time Reversal system test

7.3 Application 2: SNR Measurement

Our testbed requires an efficient real-time SNR estimation algorithm. The parameters in transmitter such as data rate and transmit power are designed to be adaptive to the SNR at the receiver. Also, we need to estimate and record SNR during our bit error rate (BER) test. These can be done in our proposed architecture, as illustrated in Fig. 7.3. DAQ is wired directly to ADC's 8 outputs. Since each channel supports sampling rate up to 50 MHz, the maximum sampling rate can be as high as 400 MHz. SNR estimation algorithms are performed by LabVIEW. Estimated SNR values are transmitted to FPGA by DAQ and displayed in the computer screen.

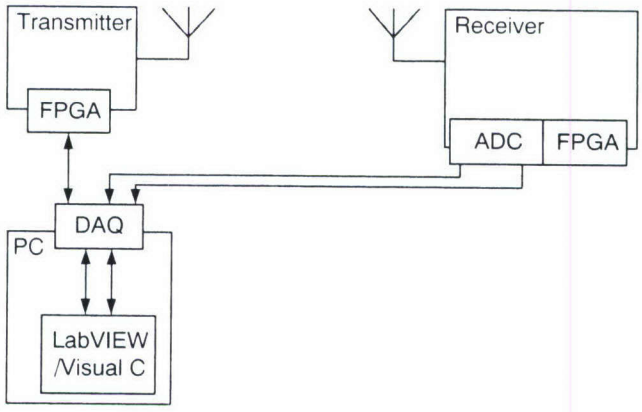

Figure 7.3: SNR test

7.4 Conclusions

This chapter introduced our proposed PC-based system testing architecture and two typical applications utilizing DSO and ADC. Other testing environments with VNA and SA can be built. Since FPGA implementation is time consuming, it is impractical to test and verify algorithm performances directly in FPGA. The testing architecture as proposed in this chapter is more desired, because programming in PC is faster and easier. Only fittest algorithms will be implemented in FPGA. In all, this architecture will increase the testing efficiency and shorten the testing period. Various testing purposes can be supported.

Chapter 8

System Verification

The testbed illustrated in Fig. 8.1 is a complete end to end UWB system with over air synchronization. The measurements are carried out in the Wireless Networking System Laboratory at Tennessee Technological University.

Listed below are instruments used for system debugging and verification:

- Tektronics Communication Signal Analyzer CSA8000B
- Tektronics Sampling module 80E03
- Tektronics Passive Probe P6109
- Tektronics Digital Phosphor Oscilloscope TDS7104
- Tektronics Logic Analyzer TLA611
- Agilent Logic Analyzer 16803A
- Agilent Function Generator 33220A
- Rohde Schwarz Signal Generator SMIQ03B
- Rohde Schwarz Spectrum Analyzer FSEM20

8.1 Measurement Results in the Transmitter

The time domain waveform shown in Fig. 8.2 is measured at the transmitter output using Communication Signal Analyzer CSA8000B with the sampling module 80E03. The amplitude of the signal is 1100 mV. The width of pulse is 4 ns. The pulse repetition frequency is 25 MHz. The signal spectrum shown in Fig. 8.3 is measured using Spectrum Analyzer FSEM20. The center frequency is 4.02 GHz. The bandwidth is 500 MHz. The maximum power level is -36.72 dBm.

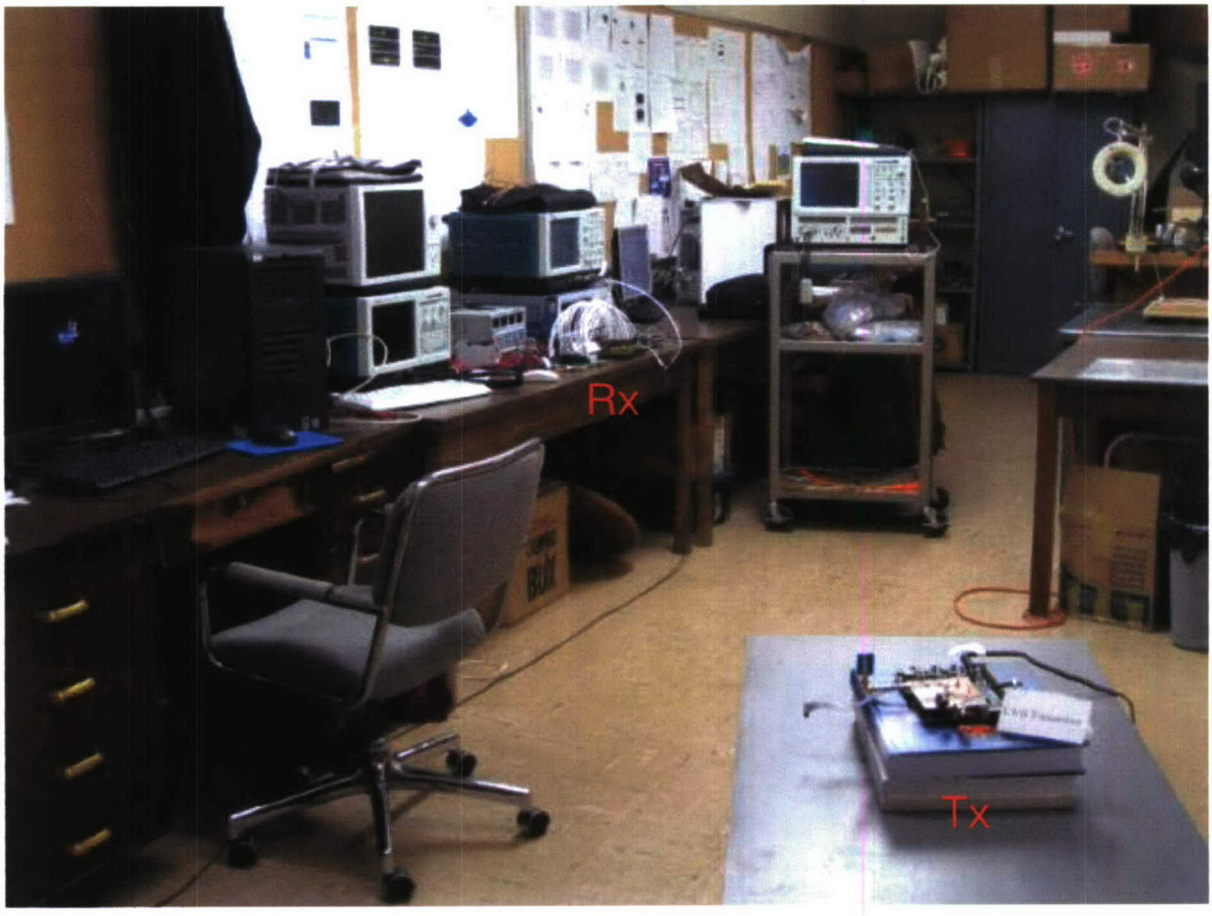

Figure 8.1: UWB testbed system

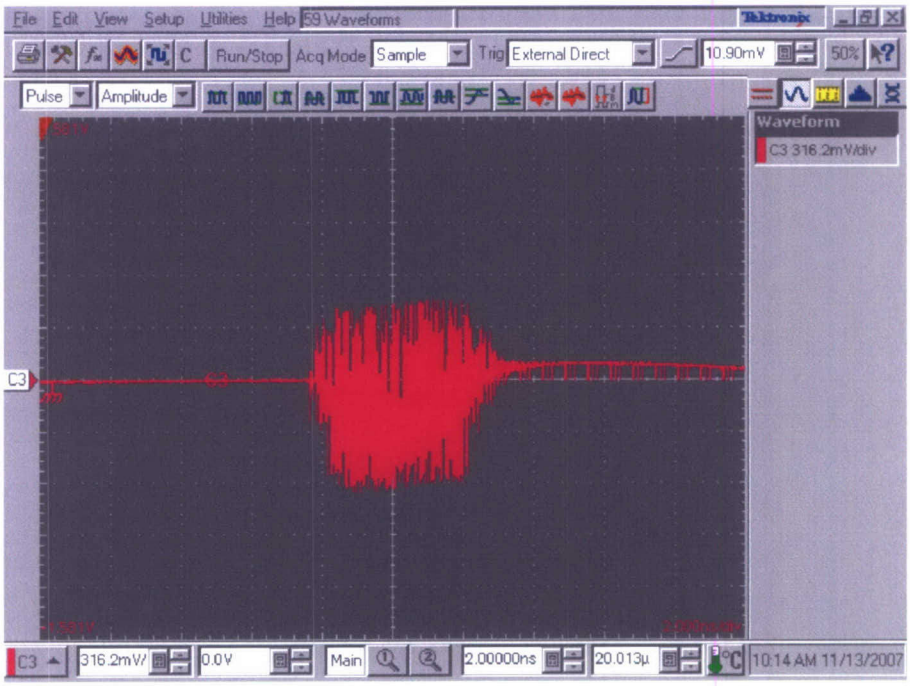

Figure 8.2: Transmitter output waveform.

8.2 Measurement Results in the Receiver

When the system is running, the output signal of the receiver shown in Fig. 8.4 can be observed by Digital Phosphor Oscilloscope TDS7104. The green signal below is the square waveform used to trigger the digital oscilloscope. The blue signal above is the output data of the receiver. It is a digital signal generated by the FPGA device. The received data pattern shown on the screen is 1010110011110000, which agrees with the transmitted data pattern. Shown in Fig. 8.5 is the receiver output captured by Logic Analyzer TLA611.

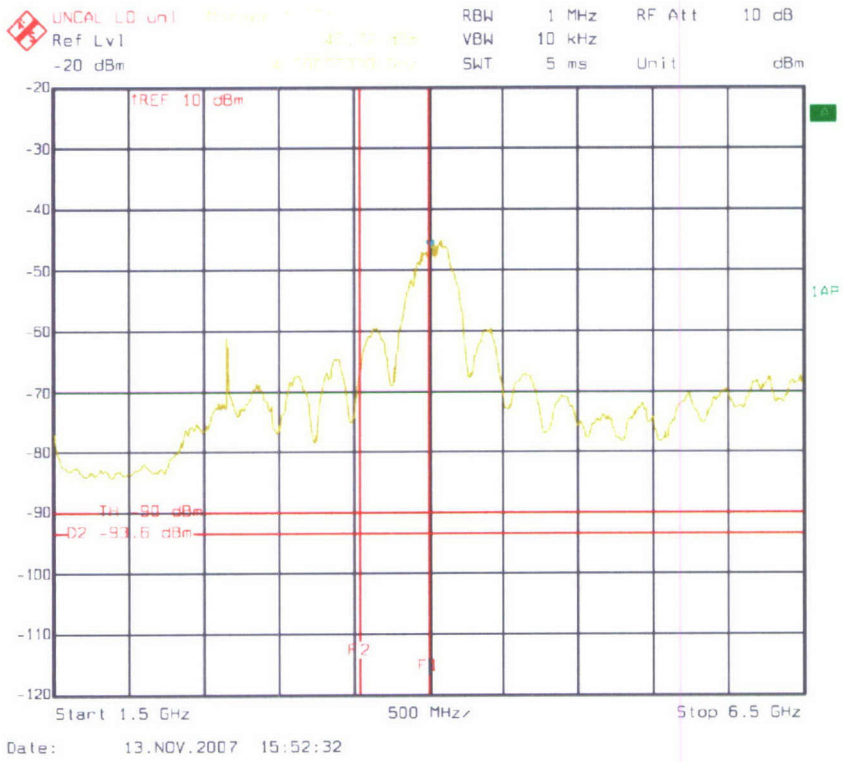

Figure 8.3: Transmitted signal spectrum.

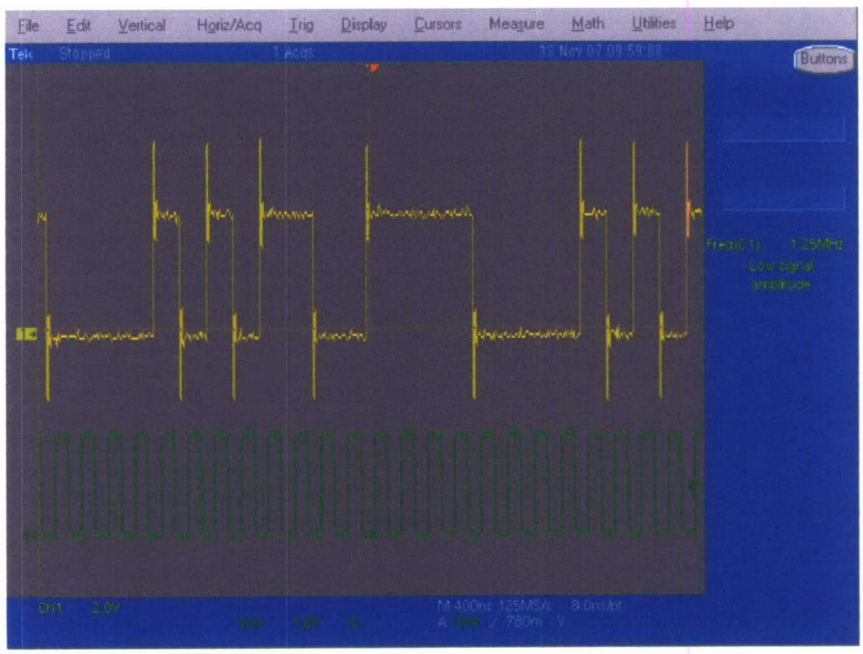

Figure 8.4: Receiver output.

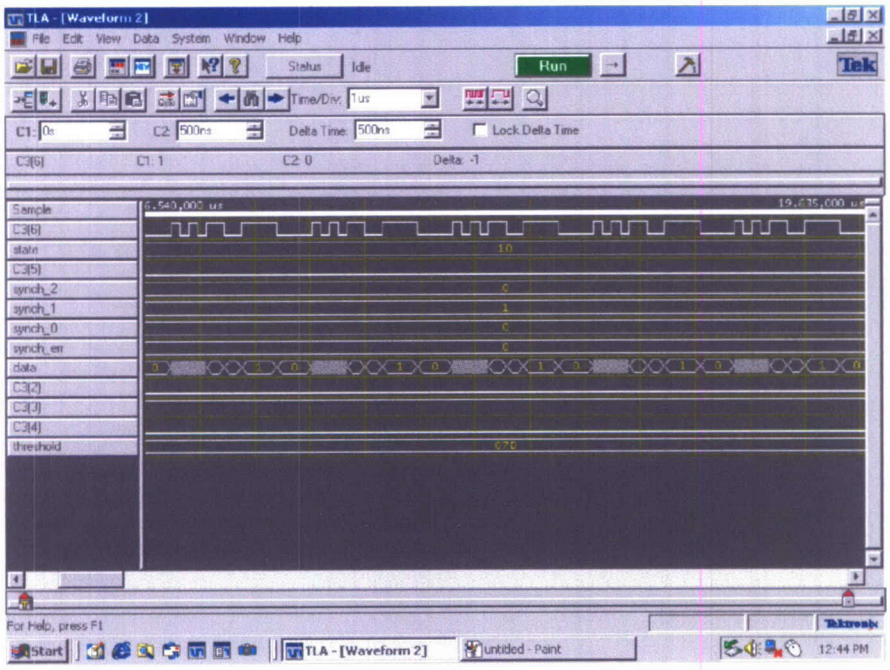

Figure 8.5: Receiver output.

8.3 System Performance

The system performance measurement is conducted in Clement Hall room 400, the Wireless Networking System Laboratory at Tennessee Technological University. The transmitter and receiver are setup in the laboratory environment with LOS. Chipscope Pro software is used to capture the receiver output data. The captured data is sent to PC to accumulate system bit-error-rate (BER). The test is performed at the distance between transmitter and receiver of 2.0 m, 2.5 m, 3.0 m, 3.5 m, and 4.0 m. Because the laboratory space is limited, a 6dB attenuator is put on the transmitter output. The equivalent distance between the transmitter and the receiver is of 4.0 m, 5.0 m, 6.0 m, 7.0 m, and 8.0 m.

Shown in Fig. 8.6 is the output data captured by Chipscope Pro in the distance of 3.5 m.

Based on the receiver output data, it has been shown that no error is observed among 20000 data at distance of 2.0 m, 2.5 m, 3.0 m, 3.5 m, and 4.0 m in the condition of successful synchronization, while the data sequence of 1010110011110000 is transmitted in the transmitter. It shows that the system can work up to 8 m without the 6 dB attenuator on the transmitter, and the testbed works on the high SNR region of the energy detector. A PN sequence will be used for BER test in the future.

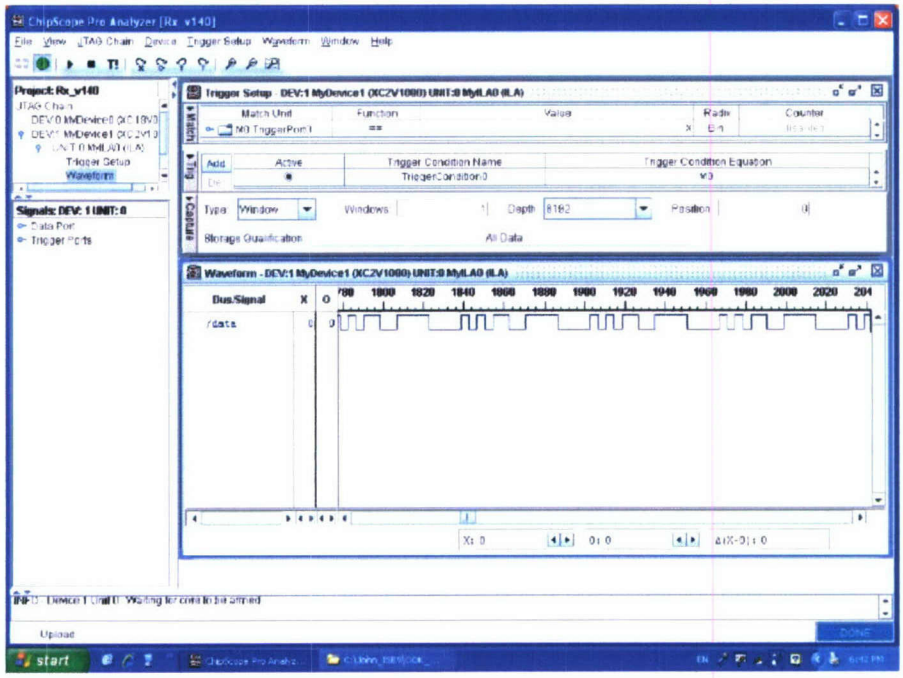

Figure 8.6: System output.

8.4 Conclusions

Based on performance test result, it can be concluded the general purpose UWB testbed works properly in the laboratory environment.